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A design concept for radiation hardened RADFET readout system for space applications

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ABSTRACT

Instruments for measuring the absorbed dose and dose rate under radiation exposure, known as radiation dosimeters, are indispensable in space missions. They are composed of radiation sensors that generate current or voltage response when exposed to ionizing radiation, and processing electronics for computing the absorbed dose and dose rate. Among a wide range of existing radiation sensors, the Radiation Sensitive Field Effect Transistors (RADFETs) have unique advantages for absorbed dose measurement, and a proven record of successful exploitation in space missions. It has been shown that the RADFETs may be also used for the dose rate monitoring. In that regard, we propose a unique design concept that supports the simultaneous operation of a single RADFET as absorbed dose and dose rate monitor. This enables to reduce the cost of implementation, since the need for other types of radiation sensors can be minimized or eliminated. For processing the RADFET's response we propose a readout system composed of analog signal conditioner (ASC) and a self-adaptive multiprocessing system-on-chip (MPSoC). The soft error rate of MPSoC is monitored in real time with embedded sensors, allowing the autonomous switching between three operating modes (high-performance, de-stress and fault-tolerant), according to the application requirements and radiation conditions.

1. Introduction

The space radiation originates from three main sources: galactic cosmic rays (GCRs), solar particle events (SPEs) and energetic particles trapped in the Earth's magnetic field (Van Allen Belts). Each of these sources may consist of different types of radiation, such as protons, neutrons, electrons, heavy ions, gamma and x-rays. The energy of space radiation covers a wide range (from keV to GeV), while the exposure rate (particle flux) can vary over several orders of magnitude during a short period of several hours or days, particularly during the SPEs [1]. Such intense radiation is harmful and potentially lethal for humans. In addition, it can cause temporary or permanent failures in electronic systems. Therefore, the monitoring of radiation exposure and the use of radiation hardened electronic equipment are key requirements for space applications. These requirements are becoming more and more critical with the increasing number of satellites in the Earth's orbit over the past few years, as well as with the emerging applications such as the Internet-of-Space and space solar energy farms.

Monitoring of ionizing radiation exposure is accomplished with the specialized electronic instruments known as radiation dosimeters. A radiation dosimeter consists of at least one radiation sensor and data processing electronics. The main function of radiation dosimeters is the measurement of total absorbed dose and dose rate under radiation exposure. Due to their small size, high sensitivity to ionizing radiation and compatibility with the standard Complementary Metal Oxide Semiconductor (CMOS) technologies, the semiconductor-based electronic and optoelectronic devices are widely used as radiation sensors, both in space and terrestrial applications. A detailed review of various radiation sensors can be found in [2–5]. One of the most widely used radiation sensors for space applications is the Radiation Sensitive Field

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Effect Transistor (RADFET). The RADFETs have substantial advantages over other types of dosimeters, as will be discussed in Section 2, and they have been operated in numerous space missions, as well as in medical, industrial and research applications [6–13].

For acquisition of the signal from the radiation sensors and subsequent computation of absorbed dose and dose rate, the mixed-signal processing is required. Depending on the application requirements, the processing can be implemented with general-purpose microcontrollers, Field Programmable Gate Arrays (FPGAs) or Application Specific Integrated circuits (ASICs). However, the electronic systems may be sensitive to ionizing radiation. The failures in electronic systems are resulting from two main radiation-induced effects: Total Ionizing Dose (TID) and Single Event Effects (SEEs). TID causes gradual degradation of transistors' electrical characteristics, eventually resulting in the change of threshold voltage, degradation of subthreshold slope, or increase of leakage current. As a result of TID-induced effects, the propagation delay of logic gates may increase, resulting in deterioration of the circuit performance. On the other hand, the SEEs are caused by the passage of a single energetic particle (e.g., a heavy ion, proton, neutron, alpha particle) through a sensitive transistor in the circuit. The most common types of SEEs are the Single Event Latchup (SEL), Single Event Transients (SETs) and Single Event Upsets (SEUs). The SEL leads to excessive supply current flow, and may result in permanent system damage if the power cycling is not applied to restore the normal operation. On the other hand, the SETs and SEUs cause temporary data corruption, known as soft errors. A detailed discussion of different types of SEEs can be found in [14, 15].

The soft errors represent the most critical cause of radiation-induced failures in modern CMOS technologies. Therefore, the design of electronic instrumentation for space missions requires special measures for soft error mitigation. However, the mitigation techniques are typically based on some form of spatial, temporal or information redundancy, which incurs significant area, power and performance penalties. Due to the variability of space radiation intensity, and limited energy resources in space, the self-adaptive fault tolerance is the optimal solution. The main idea of a self-adaptive fault-tolerant concept is to employ special radiation sensors for monitoring the Soft Error Rate (SER) of the target system, and the hardening mechanisms are activated only at critical SER levels (when high particle flux is detected). A self-adaptive system may be cost-effectively implemented with a multi-processing system-on-chip (MPSoC) that offers superior performance over a single-core system in terms of computational capacity and energy efficiency [16]. The MPSoC architecture enables to configure dynamically the on-chip processing cores into different operating modes, thus achieving a trade-off between performance, power consumption and reliability [17, 18]. Due to these benefits, the MPSoCs are attracting immense interest for data processing in space applications.

To our best knowledge, the current state-of-the-art lacks solutions for the self-adaptive RADFET dosimeters. Furthermore, the existing readout methods support only the absorbed dose measurement with the RADFET, while additional sensors (e.g., diodes) need to be employed for dose rate monitoring. In this work, we aim to propose a design concept for space radiation monitoring system by combining the best practices from RADFET dosimetry and self-adaptive fault tolerance. Specifically, this work introduces a radiation monitoring solution with the following unique features:

a) A readout method for simultaneous measurement of absorbed dose and dose rate with a single RADFET, based on successive switching between the voltage and current readout modes.
b) Use of a self-adaptive quad-core MPSoC platform as a basis of the RADFET readout system, supporting the dynamic selection of three operating modes (high performance, de-stress and fault-tolerant), according to the application requirements and system status parameters.
c) Use of sensors embedded in MPSoC for the online monitoring of particle count rate, aging, supply voltage, temperature, and clock frequency. The information from these five sensors, together with the total dose obtained from RADFET, enables to measure accurately the variation of MPSoC's SER, and accordingly select the most appropriate fault-tolerant mode.

This work is an extension of [19]. With respect to [19], this paper introduces a more detailed discussion of the system design, with block diagrams of the most important functional units. The paper also introduces an extended discussion of the preliminary design specifications, and an analytical estimate of the power consumption in space environment. In addition, a flow for the online SER monitoring is presented.

The rest of article is structured as follows. The limitations of related work and advancements offered by our concept are discussed in Section 2. In Section 3, the fundamentals of RADFET dosimetry are introduced. The proposed design of the radiation hardened RADFET readout system is presented in Section 4. The functionalities of analog and digital subsystems are discussed in Section 5 and Section 6, respectively. The preliminary design specifications for analog and digital subsystems are elaborated in Section 7. In Section 8, the online monitoring of the MPSoC's SER is discussed.

2. Related Work and Proposed Solution

2.1 Benefits and Limitations of RADFET Dosimetry

RADFET, also known as MOSFET or pMOS dosimeter, is a p-channel MOS transistor specially designed for high sensitivity to ionizing radiation. It was first reported in 1970s by *Holmes-Siedle* [20], and since then has been widely used as integrating radiation dosimeter for absorbed dose measurement. The sensing region for absorbed dose measurement is the gate oxide, which is most commonly implemented as SiO_2. The ionizing radiation causes the accumulation of positive charge in the oxide, leading to an increase of the RADFET's threshold voltage with the increase of absorbed dose.

The use of RADFETs for absorbed dose monitoring offers numerous advantages over other dosimeters. The key advantage is the possibility to operate either in active mode (with gate bias) or in passive mode (without gate bias). Operation without bias is beneficial for power saving. The RADFETs can store the dosimetric information, allowing either real-time or delayed dose reading. In contrast, alternative dosimeters based on PN and PIN diodes require continuous biasing and readout during irradiation. Furthermore, the RADFETs require simple readout circuit for threshold voltage measurement, while diodes require fast data acquisition electronics to integrate the radiation-induced current. The advantages of RADFETs also include immediate and non-destructive readout, ability to operate over a wide dose range (from several mGy to several kGy) and competitive price (around 100 Euro per RADFET and readout circuit board) [21]. Moreover, in our previous work [22], we have shown for the first time that the RADFETs can be also used for the real-time dose rate monitoring when configured as a PN junction and operated in current readout mode. The RADFETs have very small active volume and die size (typical active area is below 0.2 mm^2, while the thickness is not greater than 2 μm, and a typical die size is 1 mm^2 area and 500 μm^2 thickness), facilitating the integration into miniature sensing probes. A more detailed discussion on absorbed dose and dose rate monitoring with RADFETs is given in Section III.

However, the RADFETs have also certain limitations which must be taken into consideration when planning a particular mission. The major limitation is that the degradation process in the oxide is cumulative, which limits the total measurable dose (threshold voltage shift eventually saturates at very high doses). As a consequence, the RADFET's lifetime is limited. Nevertheless, the partial recovery and reuse of the RADFET may be possible after annealing at elevated temperature for

sufficient time. Another important issue is that the RADFETs suffer from fading effect, i.e., gradual loss of dosimetric information. However, the choice of RADFET with appropriate sensitivity can ensure its operability during the entire mission, while the real-time read-out can effectively compensate for the annealing effect. For practical applications it is also important to take into account that the RADFETs' dose readout is dependent on dose rate and energy of radiation. The dose rate dependence is particularly pronounced at low dose rates, and this effect is known as Enhanced Low Dose Rate Sensitivity (ELDRS) [23]. Therefore, the information on the dose rate is needed for correcting the measured absorbed dose value, and the calibration must be done for different types of radiation in order to account for energy dependence.

2.2 RADFET Readout Solutions for Space

Practical application of RADFETs requires customized readout electronics. Various RADFET readout systems for space missions have been reported [24 – 27]. However, these solutions have two major limitations: (i) only the absorbed dose can be monitored, (ii) radiation hardening measures cannot be adapted to dynamic radiation conditions.

Since the particle flux in space may vary over several orders of magnitude, the dose rate may also vary across a wide range. Therefore, measuring only the absorbed dose in space is not sufficient to characterize the radiation exposure. Besides, as mentioned in previous discussion, for accurate measurement of absorbed dose, it is necessary to consider the RADFET's dose rate dependence. As RADFETs have been traditionally used only for dose monitoring, additional sensors such as diodes were employed to track the dose rate changes. However, using multiple sensors of different types may require different processing elements, imposing high design costs. Since we have demonstrated in previous work the feasibility of measuring the dose rate with RADFET [22], it could be possible to use a single RADFET for measuring both the absorbed dose and dose rate.

All reported RADFET readout solutions [24 – 27] employ a single processing core in the form of a commercial microcontroller or FPGA. While a single core is generally sufficient for processing the signals from a limited number of sensors, the key limitations are related to the cost-effectiveness of radiation hardening. The radiation hardness of single-core designs is usually achieved through the static hardening, either by applying the hardware redundancy within FPGA or by using redundant microcontrollers. The static hardening introduces significant overhead in terms of power consumption, because the redundant logic is always active. Such a solution is not optimal under low radiation intensity. Thus, when the system SER is low (radiation intensity is low), it is desirable to switch off the hardening mechanisms in order to reduce the power consumption. This can be achieved with the dynamic fault tolerance. However, to the best of our knowledge, there are no public reports on the use of dynamic fault tolerance in space-grade radiation dosimeters.

2.3 Dynamic Fault Tolerance

The multiprocessing platforms implemented on a single chip, i.e., MPSoCs, are very convenient for the implementation of dynamic fault tolerance. An MPSoC contains multiple processing cores, allowing to arrange various fault-tolerant configurations by coupling the cores into redundant configurations. The use of existing on-chip resources for achieving the fault tolerance minimizes the hardware overhead, which is a typical drawback of conventional fault-tolerant techniques. Furthermore, the cores can be engaged in parallel processing when required, or switched off when intensive data processing is not necessary. As a result, the system reliability, performance and power consumption can be controlled during the runtime. Although the dynamic fault tolerance of MPSoC architectures has been widely explored, the self-awareness based on the online sensing of parameters which collaboratively affect the fault tolerance under space radiation exposure has not been addressed thoroughly in previous works.

One of the main requirements for dynamic fault tolerance is to monitor in real time the system SER variation, and accordingly apply the fault-tolerant mechanisms when the SER is high enough to affect the system's functionality. The online monitoring of SER can be accomplished with dedicated sensors for measuring various intrinsic and environmental parameters which influence the SER. The main challenge is that the SER is a complex function of multiple parameters, among which the most significant are the particle flux, total dose, temperature, supply voltage, clock frequency, and aging. An FPGA-based reconfigurable fault-tolerant architecture, with on-chip BRAM modules as particle count rate monitors, has been proposed in [1, 28]. This solution allows to reconfigure the FPGA between the high-performance mode (no fault tolerance) and the fault-tolerant mode based on triple modular redundancy (TMR). However, it does not support the measurement of other parameters which affect the SER. Another method, based on hardware-software collaborated fault tolerance in the MPSoC, has been proposed in [29]. This solution employs on-chip hardware sensors for detecting the soft error occurrence, and the software-based error correction is accordingly triggered. However, the sensors cannot detect the changes in environmental conditions which influence the SER. In [30], a reconfigurable fault-tolerant FPGA solution, supporting the connection of external radiation sensor, has been proposed. This solution enables to set the FPGA in high-performance mode (no fault tolerance) and four fault-tolerant modes: dual modular redundancy (DMR), TMR, algorithm-based fault tolerance (ABFT) and internal TMR. However, similarly to [28], the lack of on-chip sensors for monitoring the system state parameters affects the SER computation accuracy.

By neglecting any of the aforementioned parameters that affect the system SER, the error in SER computation may be even beyond 100 %. The increase of particle flux results in a linear increase of the system SER [31], and this dependence is especially critical because the particle flux in space can vary over several orders of magnitude. By neglecting the impact of temperature variations, the computed SER for combinational logic may deviate by 145 % from the actual value when temperature increases from 25 to 100 °C [32]. Similarly, neglecting the impact of supply voltage fluctuations may cause up to 152 % inaccuracy in the SER [33]. Due to aging effect, the SER of SRAM may vary by more than 30 % over five years [34]. The TID of 15000 Gy (1500 krad) leads to an increase of SER by 170 %, but as TID increases beyond 15000 Gy (1500 krad) the SER decreases [35]. As both aging and TID cause the change of transistors' threshold voltage, it is important to distinguish the contribution of these two effects. Moreover, the combinational SER increases linearly with clock frequency, and at clock frequencies in the GHz range the SER of certain combinational circuits may be comparable to that of sequential circuits [36].

2.4 Proposed Solution

In comparison to previous RADFET readout solutions [24-27], this work is the first to propose the use of RADFET for the simultaneous measurement of absorbed dose and dose rate. This is achieved with the analog switching between the total dose and dose rate reading modes. Such an approach enables to obtain detailed information on the radiation exposure in real time using a single radiation sensor. As a result, the overall implementation cost can be minimized, while leveraging the unique benefits of the RADFET dosimetry. The information on the dose rate also allows to take into account the ELDRS effect, and provide accurate absorbed dose computation under variable dose rates.

The proposed readout system is based on a self-adaptive quad-core MPSoC with a support for the real-time tracking of its SER in terms of the status parameters monitored with embedded sensors. The basis of the proposed design are the custom-designed framework controller for managing the MPSoC operation, and the Static Random Access Memory (SRAM) for data storage and particle count rate monitoring. Additional sensors for monitoring the supply voltage variation, temperature and

aging are embedded in the system to provide a comprehensive system state monitoring. Such a solution allows for dynamic selection of the operating and fault-tolerant modes according to the workload, system status and measured radiation intensity. As a result, higher integration level and flexibility compared to the state-of-the-art RADFET readout solutions can be achieved. In comparison to previous reconfigurable fault-tolerant architectures [28, 30], our solution does not support only the particle count rate monitoring, but also the monitoring of total dose and additional system parameters, thus allowing to achieve better accuracy in SER computation.

The functionality of the MPSoC is not limited to monitoring of one or more RADFETs, but it is also possible to monitor other types of sensors within a spacecraft/satellite. Moreover, the same platform can perform other mission-critical tasks (e.g., navigation, image processing, communication). Such a hybrid concept is crucial in space applications where high level of integration and fault tolerance with minimum power consumption are required.

3. Measurement of Absorbed Dose and Dose Rate with RADFET

3.1 RADFET as Absorbed Dose Monitor

The underlying principle of absorbed dose measurement with the RADFET is the conversion of the threshold voltage shift, ΔV_T, resulting from radiation-induced charge, into the absorbed dose, D. When the RADFET is exposed to ionizing radiation, the electrons and holes are created in the device as a result of ionization process. Most of the released electrons quickly leave the oxide and they do not contribute to the threshold voltage shift. The charge carriers that cause the threshold voltage shift are the holes generated in the gate oxide, and the traps at the very interface between oxide and substrate (bulk), as illustrated in Fig. 1.

The dependence of threshold voltage shift on absorbed dose is usually expressed with the power relation:

$$\Delta V_T = S \cdot D^n \tag{1}$$

where S is a fitting constant representing the sensitivity, and n is the degree of linearity. Typical sensitivity is from tens to hundreds of mV/Gy. The value of n is ideally 1 (indicating perfect linearity), but in practice it varies from 0.6 to 0.98. A typical calibration curve for a RADFET sample is illustrated in Fig. 2 [37].

Although relation (1) is widely used in practice, it neglects some major physical mechanisms, and therefore can lead to inaccurate calculation of very high absorbed doses. Namely, according to relation (1), ΔV_T will increase monotonically as D increases. This means that for an assumed infinite value of D, ΔV_T will also be infinite. However, this is not physically possible because the volume of the oxide is finite, and hence the electric field and the defect density in the oxide are also finite. Based on this reasoning, an improved model for calculating the absorbed dose from the threshold voltage shift has been proposed and experimentally verified [38],

$$\Delta V_T = a - \frac{a}{1 + b \cdot D^c} \tag{2}$$

where a, b and c are constants for a given RADFET obtained by fitting the experimental results. As elaborated in [38], the fitting coefficients are almost invariant with the number of fitting points. This means that only few radiation points are sufficient to obtain the fitting coefficients, which is significant from the application point of view.

When used for absorbed dose monitoring, two operating modes for RADFET have to be distinguished: (i) sense mode (irradiation mode, with no readout done), and (ii) readout mode. In the "sense" mode the RADFET is exposed to irradiation, either without bias or with applied bias. If gate bias is not applied, all pins are grounded. On the other hand, in the readout mode, the absorbed dose measurement is performed with a readout circuit illustrated in Fig. 3. A constant current (typically of the order of tens of μA) is supplied through the drain, and the threshold voltage is measured between the drain and ground. It is important to note that the readout is sensitive to ambient temperature. Therefore, it is necessary to monitor the temperature and take into account the temperature variations in dose computation.

The sensitivity S for absorbed dose measurement is largely determined by the gate oxide thickness and the applied gate bias voltage. In general, thicker gate oxide and higher positive gate bias voltage result in higher sensitivity. Typical oxide thickness is in the range from 100 nm to several μm, and the bias voltage of several volts can provide the increase in sensitivity of more than 50 % compared to the zero-bias mode. However, both approaches have limitations. The possibility of increasing the bias voltage is limited by the electric field which the device can withstand. On the other hand, the use of thicker oxides has also a limitation in terms of readout stability. Alternatively, the stacking of multiple RADFETs [39] can be employed to obtain higher sensitivity. In the past several years, the use of new materials for substrate and oxide

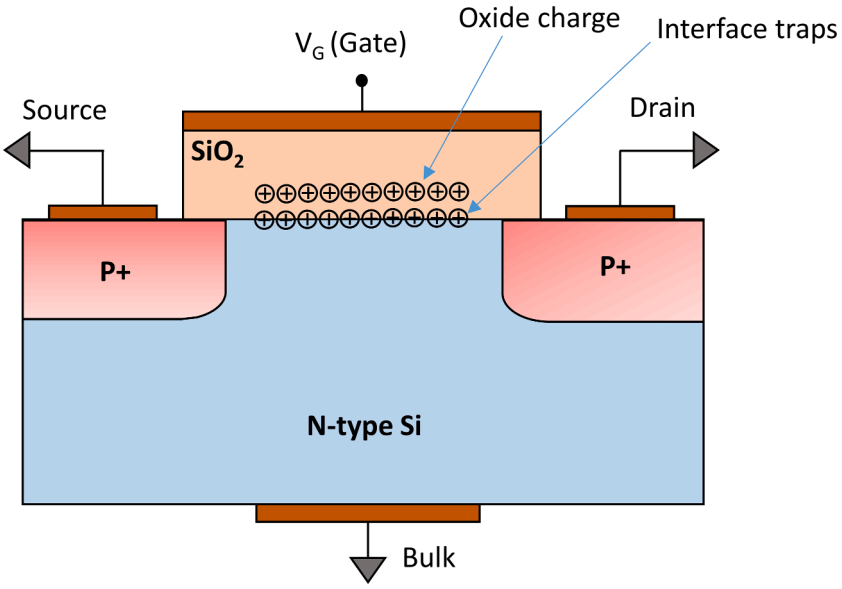

Fig. 1. RADFET cross-section illustrating the radiation-induced charge deposition in the oxide

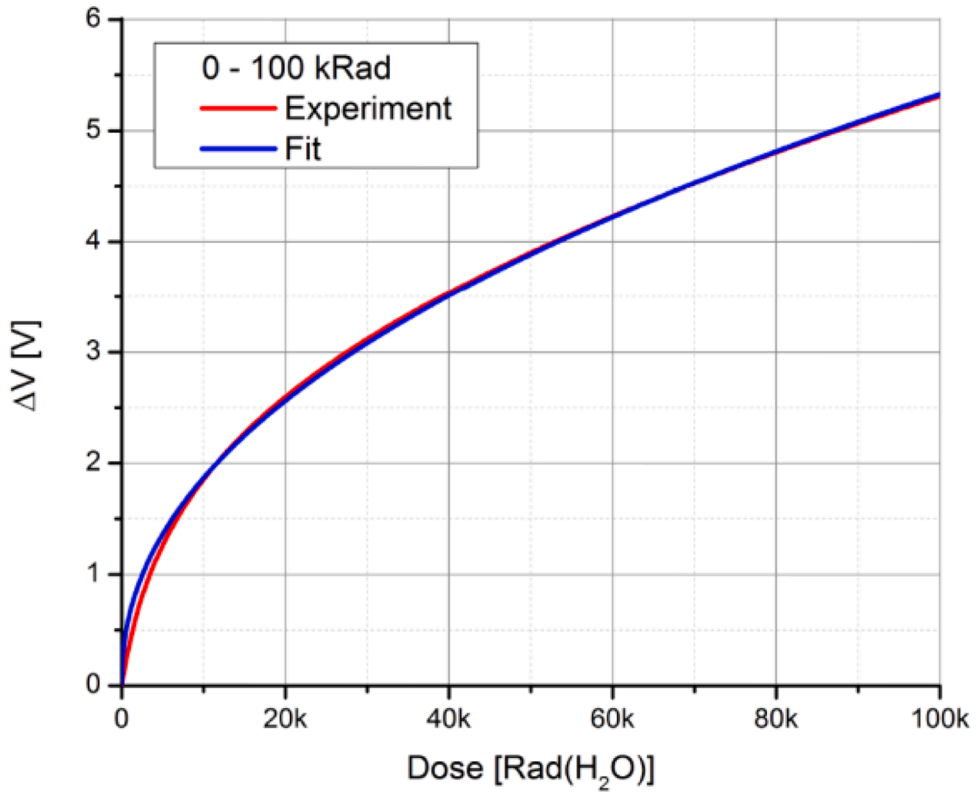

Fig. 2. Typical RADFET calibration curve obtained with Co-60 gamma irradiation at dose rate of 50 Gy/h and room temperature [37]

has shown very promising potential for achieving higher sensitivity [40-42].

3.2 RADFET as Dose Rate Monitor

The possibility of using the RADFETs for the dose rate monitoring has been demonstrated experimentally (with Co^{60} gamma radiation) [22]. In contrast to the absorbed dose measurement approach where the gate oxide is the sensitive area, for dose rate measurement the substrate (bulk) is the sensing region. As a result of radiation exposure, free electron-hole pairs are generated in the substrate (as depicted in Fig. 4), and if sufficient reverse bias voltage is applied, the radiation-induced current flowing through the bulk can be measured. Therefore, by measuring successively the threshold voltage and current, the information on both total dose and dose rate can be obtained. To achieve that, an appropriate mechanism for switching between the two read-out modes has to be applied.

The dose rate measurement with RADFET [22] is performed similarly as with PN diodes, i.e., a RADFET is configured as a diode by connecting the gate, source and drain terminals to ground, while bulk is connected to positive voltage in order to provide reverse bias, as depicted in Fig. 5. Our experimental results have shown that with the reverse bias voltage from 10 to 30 V, the current induced by gamma radiation is stable during a fixed dose rate exposure, for the dose rates from 0.65 to 32 Gy/h. Depending on the reverse bias voltage, the induced current varied from around 200 pA to almost 4 nA in the investigated dose rate range. A sample of experimental results for 10 V bias is illustrated in Fig. 6.

Based on the experimental results, the mean radiation-induced current can be expressed as a function of dose rate using a power law,

$$I = k \cdot \dot{D}^m \tag{3}$$

where I is the mean effective radiation-induced current in nA, $\dot{D}$ is the dose rate in Gy/h, k is the sensitivity coefficient and m is the linearity coefficient.

The current readout sensitivity increases almost linearly with the reverse bias voltage V_{BIAS} [22]. This can be explained by the increase of the depletion layer width and the electrical field intensity within the device, resulting in more efficient charge collection, and thus in higher radiation-induced current. To take into account the impact of reverse bias voltage, an empirical relation for the induced current in terms of dose rate and bias voltage can be expressed as [22],

$$I = n \cdot V_{BIAS} \cdot \dot{D}^m \tag{4}$$

where n is determined as the quotient of parameter k in relation (3) and bias voltage V_{BIAS}. The current dependence on dose rate, for 10 and 30 V bias voltages, is illustrated in Fig. 7.

Kulhar et al. [43] have shown that the RADFETs can be also operated in the pulsed current mode, enabling to measure dose rates in the range of mGy/h. At lower dose rates, the radiation may induce individual current pulses, where the pulse count rate is proportional to dose rate. Using Co^{60} gamma radiation source, with the reverse bias voltage up to 20 V, they have measured the dose rates from 0.5 mGy/h to 10 Gy/h with very good accuracy, and demonstrated a linear dependence between pulse count rate and dose rate. Similarly to the current mode, the sensitivity in the pulse mode readout is proportional to the applied reverse bias voltage. However, the maximum measurable dose rate in the pulse mode is limited by the dead time of the measurement system (i.e., the processing time).

4. Readout System Design

Although it is possible to integrate complete processing electronics (analog and digital) in the same chip, we have decided to realize the analog and digital subsystems as separate units. This approach has been chosen because most digital elements and the analog-to-digital converter (ADC) have been verified on different chips designed at the IHP – Institute for High Performance Microelectronics. Moreover, at this

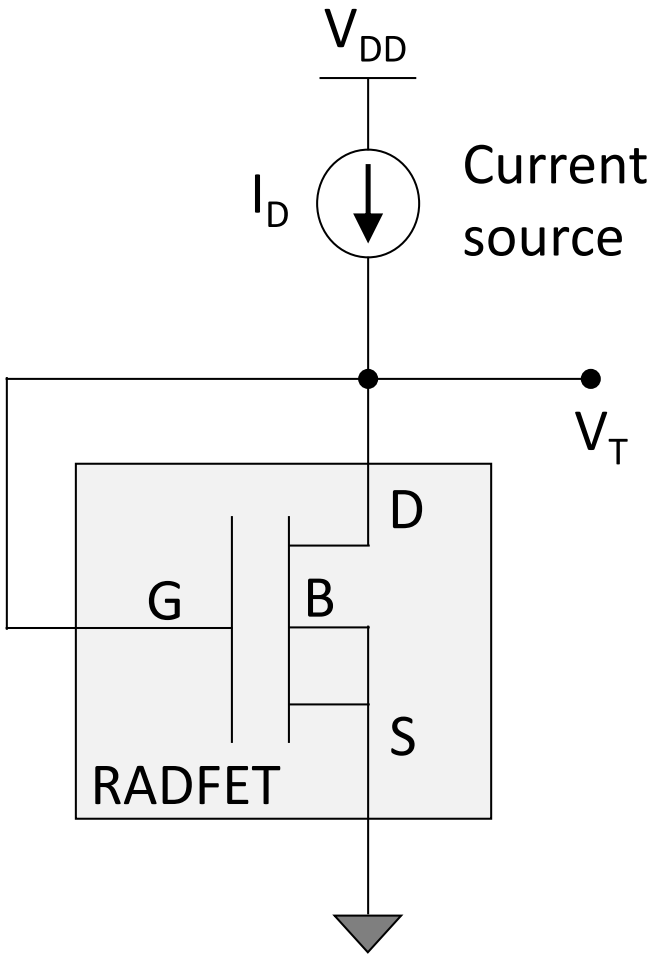

Fig. 3. Readout configuration for dose measurement

initial design stage it would be challenging to plan the on-chip integration of highly sensitive analog circuitry for measuring very low currents. It could also be possible to integrate the RADFET with the processing electronics, but then it would not be possible to replace the RADFET, and thus the whole system would have limited lifetime depending on the total dose that can be measured by the RADFET.

The proposed RADFET readout platform is composed of two main units: Analog Signal Conditioner (ASC) and a self-adaptive Multi-processor System-on-Chip (MPSoC). The block diagram of the system is illustrated in Fig. 8. The ASC is envisioned as a fully analog subsystem based on commercially available components. On the other hand, the MPSoC will be implemented on a single chip, leveraging the IHP-proprietary radiation-hardening-by-design solutions, and the IHP's 130 nm CMOS technology.

The RADFET readout system supports three main operating modes:

a) ***Sense Mode***: All pins are grounded and the RADFET is operated as absorbed dose meter, with or without bias applied to the gate terminal. Dose rate monitoring is not possible in this mode.
b) ***Absorbed Dose Readout Mode***: The voltage measurement circuit is connected to the RADFET and absorbed dose is calculated based on the threshold voltage shift (with the setup in Fig. 3).
c) ***Dose Rate Readout Mode***: The current measurement circuit is connected to the RADFET and the dose rate is calculated from the measured current (with the setup in Fig. 5).

5. Analog Signal Conditioner (ASC)

The Analog Signal Conditioner (ASC) performs initial processing of the current and voltage signals from the RADFET. It is composed of two readout channels (voltage readout channel for absorbed dose measurement, and current readout channel for dose rate measurement), and a switching matrix for selecting the readout mode. In Fig. 9, a block diagram of the ASC is illustrated. At this conceptual design stage, the idea is to implement the ASC subsystem with commercial radiation-tolerant components. In the following, the design and functional characteristics of the ASC are discussed.

5.1 Voltage Readout Channel

The voltage readout channel measures the RADFET's threshold voltage when the *Absorbed Dose Readout* mode is activated, according to the setup depicted in Fig. 3. It is made of a current source, a voltage source and a voltage measurement unit (cascaded amplifiers), as depicted in Fig. 9. The current source provides constant current bias at the drain terminal of RADFET, while the amplifier provides the required gain of the threshold voltage. The voltage source is employed for

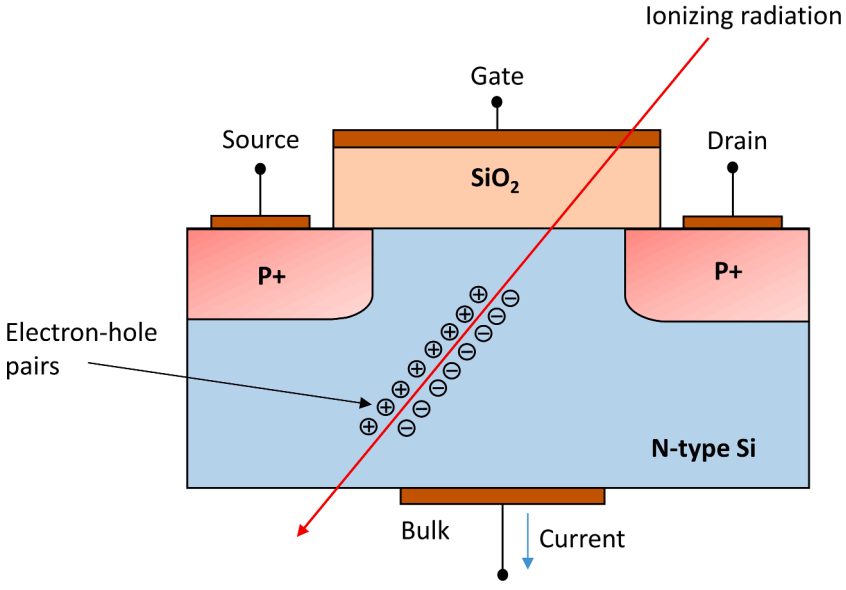

Fig. 4. RADFET cross-section illustrating the creation of electron-hole pairs in the bulk

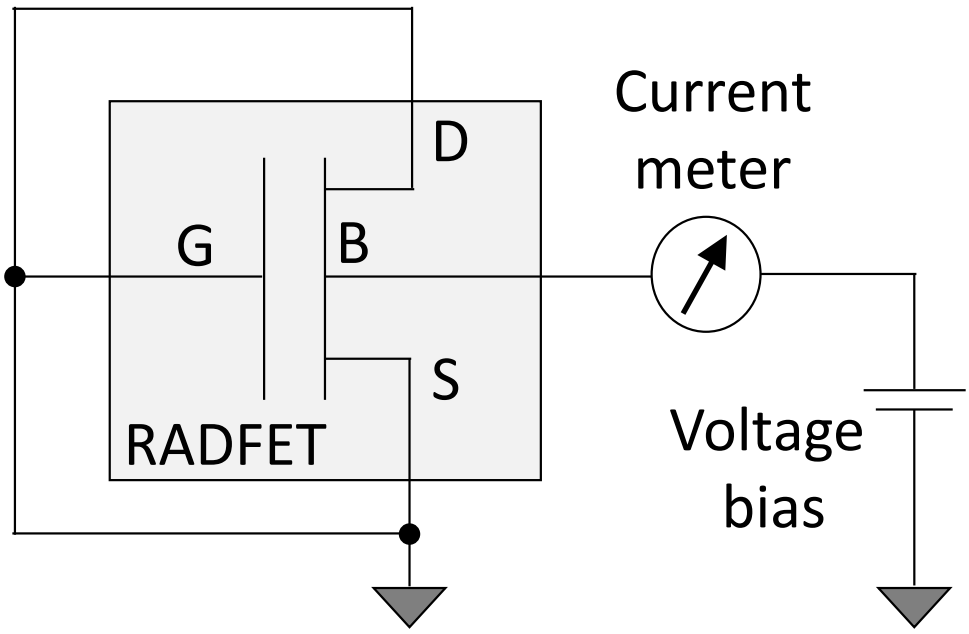

Fig. 5. Readout configuration for dose rate measurement

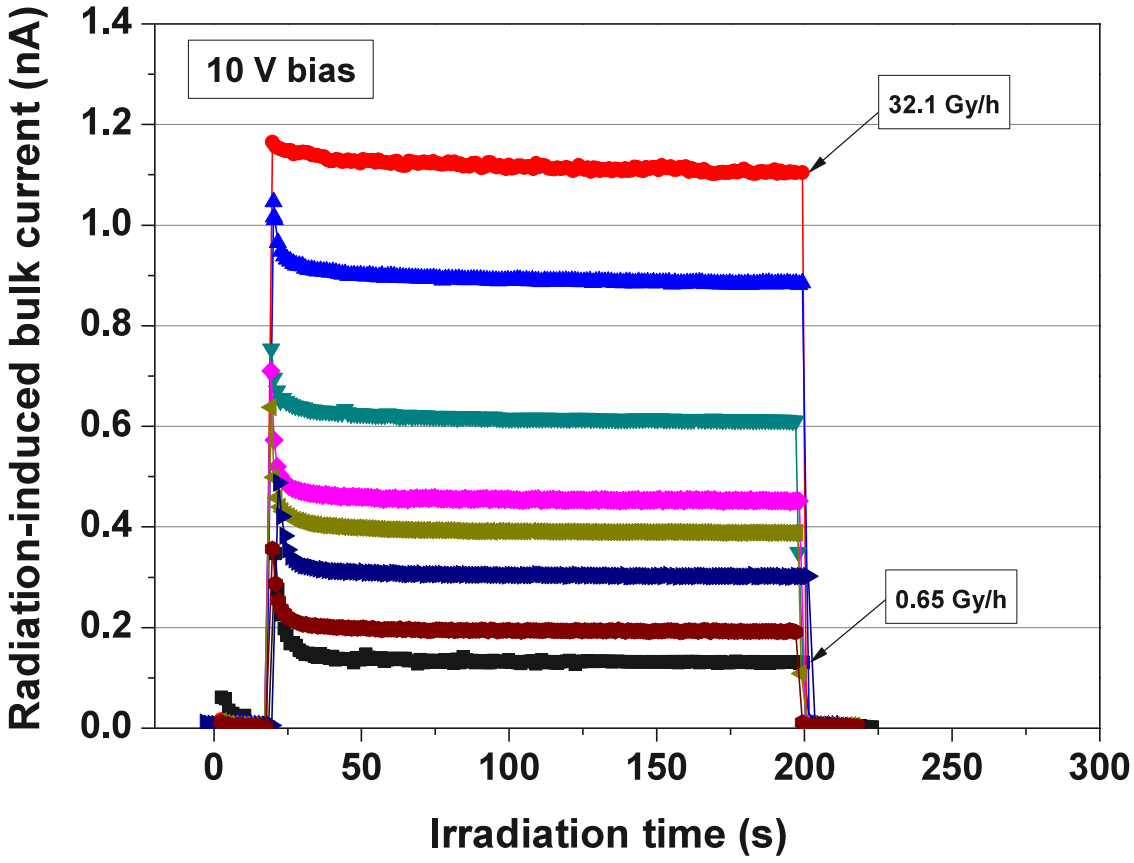

Fig. 6. Radiation-induced current in RADFET for different dose rates and bias voltage of 10 V

optional biasing of the RADFET's gate terminal, in order to control its sensitivity to radiation. Both current and voltage sources are programmable via the control signals from MPSoC. Programmability of the current source is required to adjust the current according to the temperature variations. On the other hand, programmability of the voltage source allows to adjust the sensitivity of RADFET in real time. In order to enable the measurement of threshold voltage over a wide range, a multi-range amplifier is utilized to convert the voltage from the RADFET to the voltage levels compatible with the ADC in the MPSoC. The use of a multi-range amplifier, where a wide voltage range is divided into multiple narrow voltage ranges, allows to employ the operational amplifiers with lower supply voltage (up to 5 V), thus enabling to reduce the power

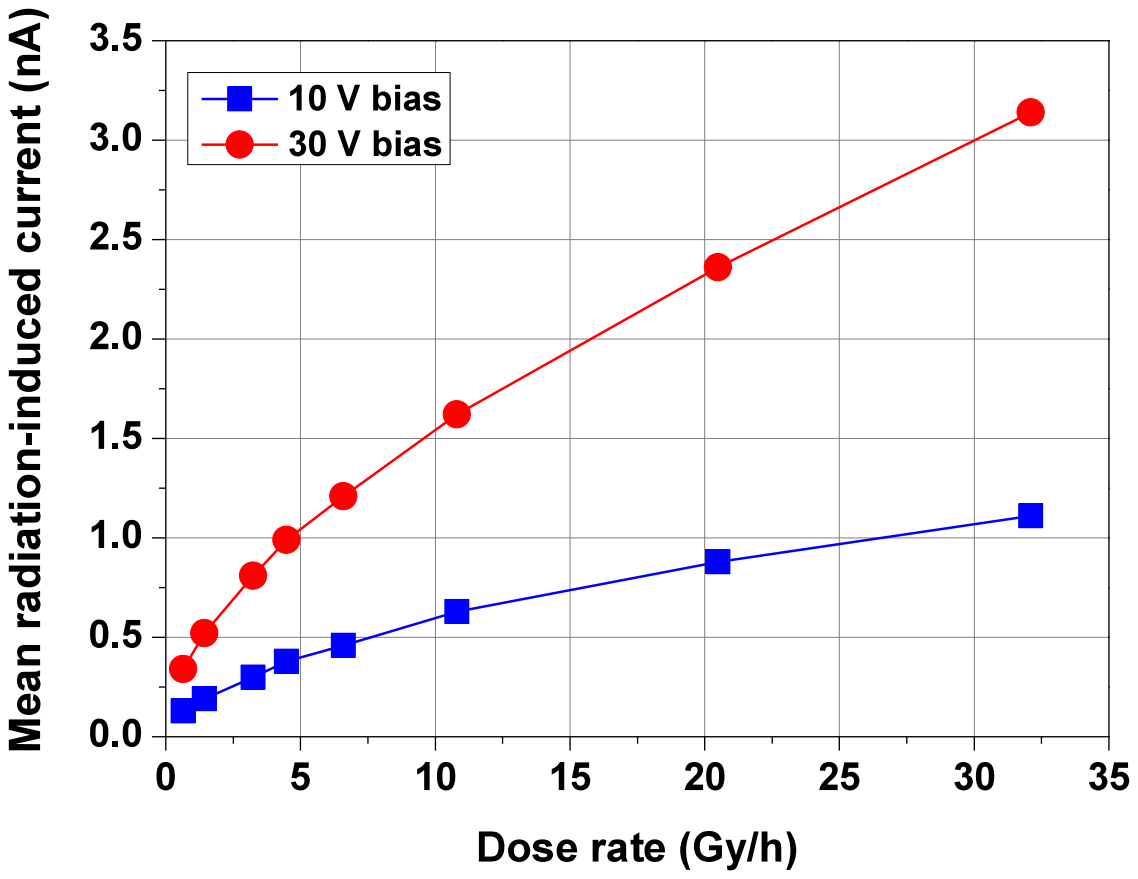

Fig. 7. Mean radiation-induced current in RADFET for different dose rates and bias voltages of 10 and 30 V

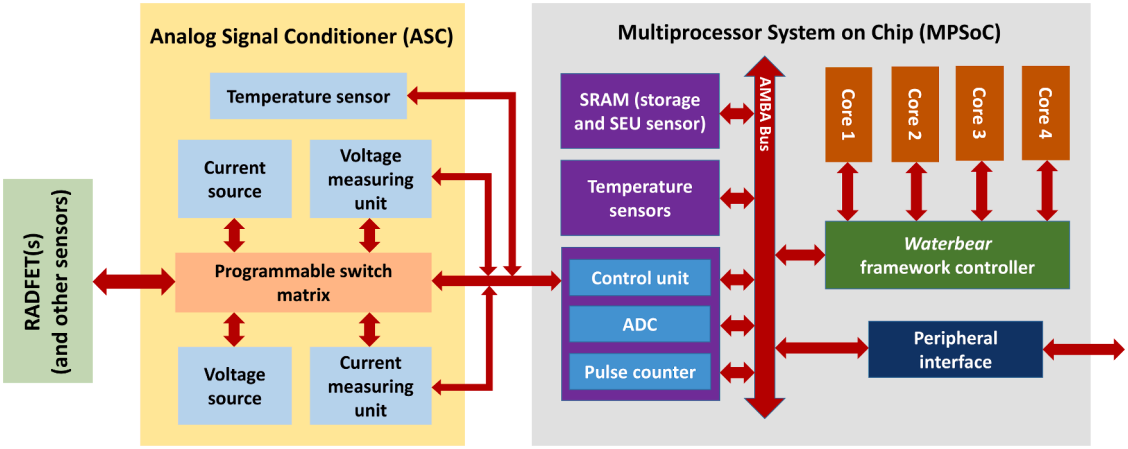

Fig. 8. Conceptual design of a radiation hardened RADFET dosimeter supporting the simultaneous measurement of absorbed dose and dose rate

consumption.

5.2 Current Readout Channel

The current readout channel performs the current measurement in the *Dose Rate Readout* mode, according to the setup shown in Fig. 5. A block diagram of the current measuring unit is depicted in Fig. 10. It consists of two units: direct current measurement unit and pulsed current measurement unit. The direct current measurement unit allows the measurement of direct current at high dose rate. It consists of a transimpedance amplifier (for converting direct current into voltage) and an additional gain stage. Due to a wide range of current that can be induced in the RADFET during radiation exposure, a multi-range transimpedance amplifier is employed. On the other hand, the pulsed current measurement unit converts the current pulses (induced at low dose rate) into voltage pulses. This is done with a charge sensitive amplifier (converts the current pulses into voltage pulses), a pulse shaping circuit, and a comparator with a fixed threshold level. For the predefined threshold level of the comparator, all pulses with amplitude above that level will be detected.

5.3 Programmable Switching Matrix

The switching matrix enables to select one of the three readout

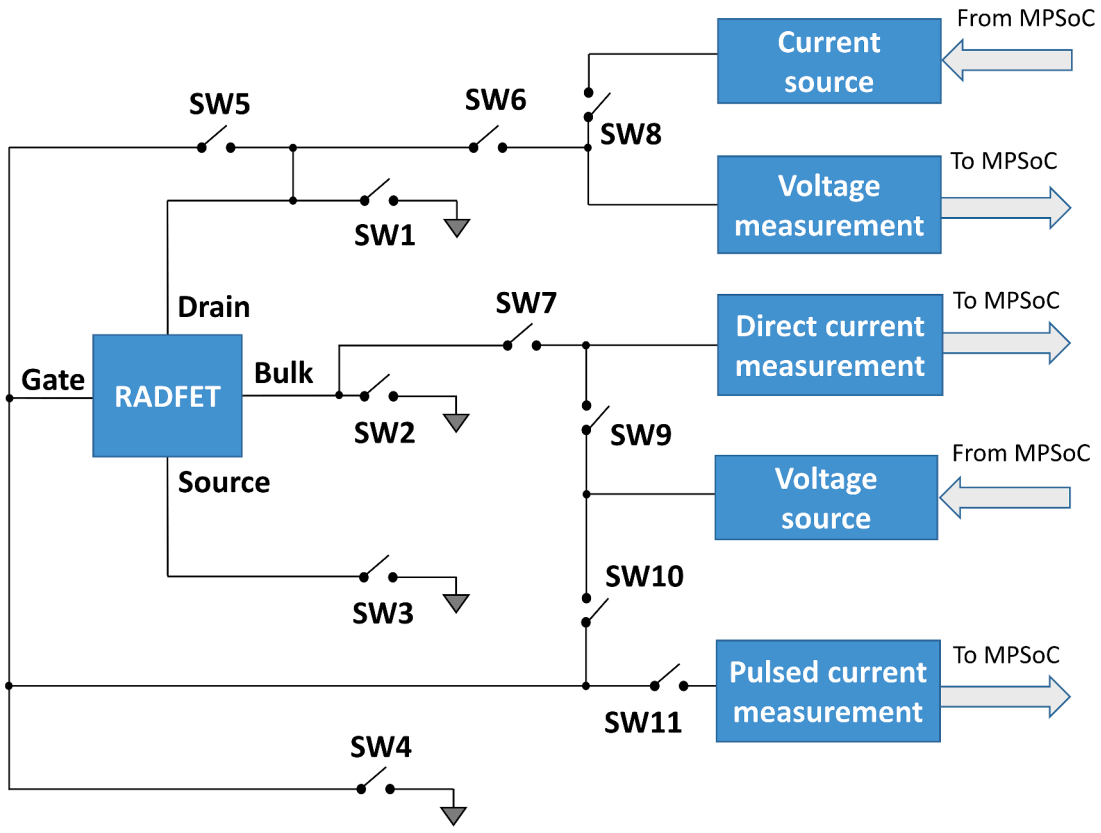

Fig. 9. ASC with interface to the RADFET (all switches are controlled by MPSoC)

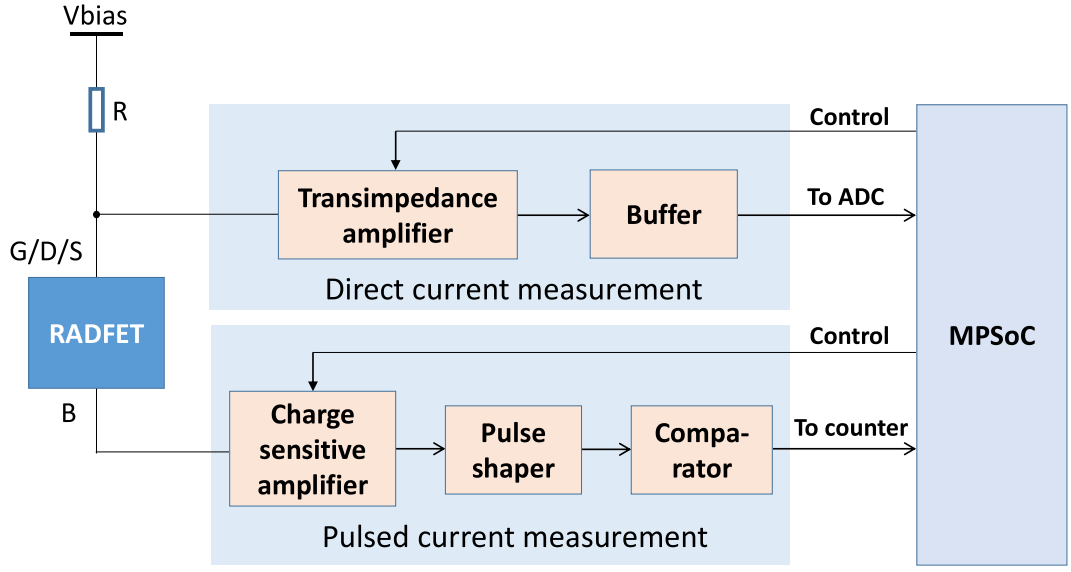

Fig. 10. Current readout circuit with interface to MPSoC

modes. It consists of 11 analog switches as illustrated in Fig. 9. The states of the switches are controlled by the digital signals from the MPSoC. The switching pattern, i.e., the time allocated to each readout mode, is defined by the program executed by the MPSoC. In Table 1, the switches used for setting each readout mode are given.

Table 1
Operating modes and corresponding switches

Readout mode	Active (closed) switches
Sense mode (without bias)	SW1, SW2, SW3, SW4
Sense mode (with bias)	SW1, SW2, SW3, SW10
Absorbed dose readout	SW2, SW3, SW5, SW6, SW8
Dose rate readout	SW1, SW3, SW7, SW9, SW11

5.4 Temperature Sensor

The RADFET's absorbed dose readout is dependent on ambient

temperature. Therefore, it is necessary to provide continuous temperature monitoring for the online calibration of dose readout. As the ambient temperature in space may vary over a wide range, one of the most suitable sensors is the platinum resistive thermometer Pt100, which can measure the temperature from -200 to 800 °C. The Pt100 temperature sensor is interfaced to the analog-to-digital converter embedded in the MPSoC.

5.5 Radiation Hardening Measures for Analog Elements

The analog circuitry may be sensitive to TID, SET and SEL. Hence, the analog components have to be chosen to comply with the required TID, SET and SEL limits. To this end, it is necessary to perform exhaustive radiation tests to verify their robustness to TID and SEE. For many space missions, typical requirements are TID tolerance up to 1000 Gy (100 krad), and SEL tolerance > 60 MeVcm^{2}mg^{-1}. Special analog components tolerant to SEL and certain TID levels are available on the market, but they are very expensive. If general purpose commercial components are chosen, their SEL, SET and TID tolerance must be verified experimentally. The TID tolerance can be improved with appropriate shielding, while the SET and SEL tolerance can be enhanced with special design techniques. The typical duration of SET pulses in analog circuits is in the range of microseconds. To mitigate the SET effects, passive filters have to be inserted at the outputs of all analog integrated circuits. For SEL protection, the current sensors are employed to detect the abrupt rise in supply current, and a watchdog timer is used to reset the power supply when excessive current is detected.

6. Self-Adaptive Multiprocessor System-on-Chip (MPSoC)

The processing platform is a self-adaptive Multiprocessing System-on-Chip (MPSoC) with four cores. It performs three functions: (i) switching between the three RADFET readout modes, (ii) control of voltage and current readout channels in ASC, and (iii) processing of data from ASC for absorbed dose and dose rate computation. The platform supports the autonomous selection of operating and fault-tolerant modes of the MPSoC during the runtime. This is achieved with a set of on-chip sensors for the real time monitoring of the MPSoC's SER. In the following, the functionality of the constitutive elements of MPSoC are described.

6.1 Waterbear Framework Controller

The basis of the self-adaptive MPSoC is the *Waterbear* framework controller, proposed in [17, 44]. It sets the MPSoC into one of three operating modes according to the application requirements and the system state. Thus, a trade-off between performance, power consumption and fault tolerance can be maintained in real time. The following operating modes may be activated when an application request is issued:

a) **High-performance mode**: the multiprocessor operates as a standard multiprocessor, i.e., each core executes its own tasks.
b) **De-stress mode**: a single core is operating while other cores are clocked- or powered-off to reduce aging and save power. Using the aging sensors embedded in each core [61], and the anti-aging technique known as Youngest-First Round-Robin (YFRR) core gating [45], the operating core is de-stressed by transferring the workload to a resting core. By destressing the cores, their lifetime is increased, which is important in long-term space missions.
c) **Fault-tolerant mode**: the cores are arranged into various N-modular-redundancy (NMR) configurations such that the coupled cores are executing the same tasks. This mode provides enhanced fault-tolerance, and the NMR configuration is chosen based on the measured SER.

The *Waterbear* framework controller is a custom-designed unit composed of three main elements: (i) a programmable majority voter for selection of NMR configurations, (ii) a set of registers for storing the control and status data, and (iii) generators for power gating (PG), clock gating (CG), interrupt and reset signals. A block diagram of the controller is illustrated in Fig. 11, and detailed explanation of all elements can be found in [44]. The functionality of the *Waterbear* framework controller has been verified on several chips, where the most representative is the PISA chip (Power-robust Microprocessor for Space) [17].

The fault-tolerant NMR configurations are selected based on the MPSoC's SER, which is determined from the reading of radiation sensors and system status monitors. The voting is performed in each cycle by a voter, which initiates the actions when the mismatch between the core outputs is detected. Three core-level fault-tolerant modes can be selected: DMR, TMR and Quadruple Modular Redundancy (QMR). The incurred area overhead is minimum, and it is related only to the added voting mechanisms. That is because the processing cores are viewed as redundant only in the fault-tolerant mode, while in the other two modes (high performance and de-stress) they are either involved in multi-processing or powered-off.

In NMR configurations, the voting unit would be a single point of failure if adequate protection is not applied. Although the voters generally have much smaller area that the cores, and thus their failure rate is much lower, it is still necessary to provide the fault-tolerant voting in order to ensure correct operation of the system. To this end, we employ a fault-tolerant voter with integrated self-checking functionality [46]. If an error occurs in the voter, an alarm signal will be generated. The error in the voter is detected by comparing the input and output signals. In the case of an error, the error correction procedure will be initiated, and the voting will be repeated in the next clock cycle.

6.2 Processing Cores

Four LEON2 cores are selected for data processing. The cores are based on 32-bit SPARC V8 architecture and AMBA 2.0 interconnection. The LEON2 processor [47, 48] is highly configurable, allowing the user to customize it for a target technology or a particular application (e.g., selecting different cache sizes, multiplier performance, clock generation, etc.). It is available as an open core in the form of a VHDL model describing the processor core, system bus and peripheral components. A graphical configuration tool based on UNIX kernel scripts is used to configure the system. The LEON2 cores are also available in fault-tolerant versions denoted as LEON2-FT, with applied triple modular redundancy for all flip-flops and error detection and correction for memory [48]. More advanced versions (LEON3, LEON4 and LEON5) are also available.

6.3 Readout Interface

The MPSoC is interfaced to the ASC through the readout interface composed of analog-to-digital converter (ADC), pulse counter and control unit. The ADC is used to digitize the analog voltage from the outputs of voltage readout channel, direct current readout channel, and Pt100 sensor. The pulse counter measures the count rate of the voltage pulses from the pulsed current readout stage. The control unit provides a set of digital control signals via the General Purpose Input/Output (GPIO) pins, for selecting the switches in the switching matrix, adjusting the measurement ranges in the current and voltage readout channels, and controlling the voltage and current bias sources.

6.4 SRAM as Data Storage Medium and SEU Sensor

For particle flux monitoring, a data-storage SRAM in the MPSoC is utilized. This unique concept of using an embedded SRAM both as data storage medium and SEU sensor has been proposed in [49]. In comparison with the stand-alone SRAM particle detectors, the proposed

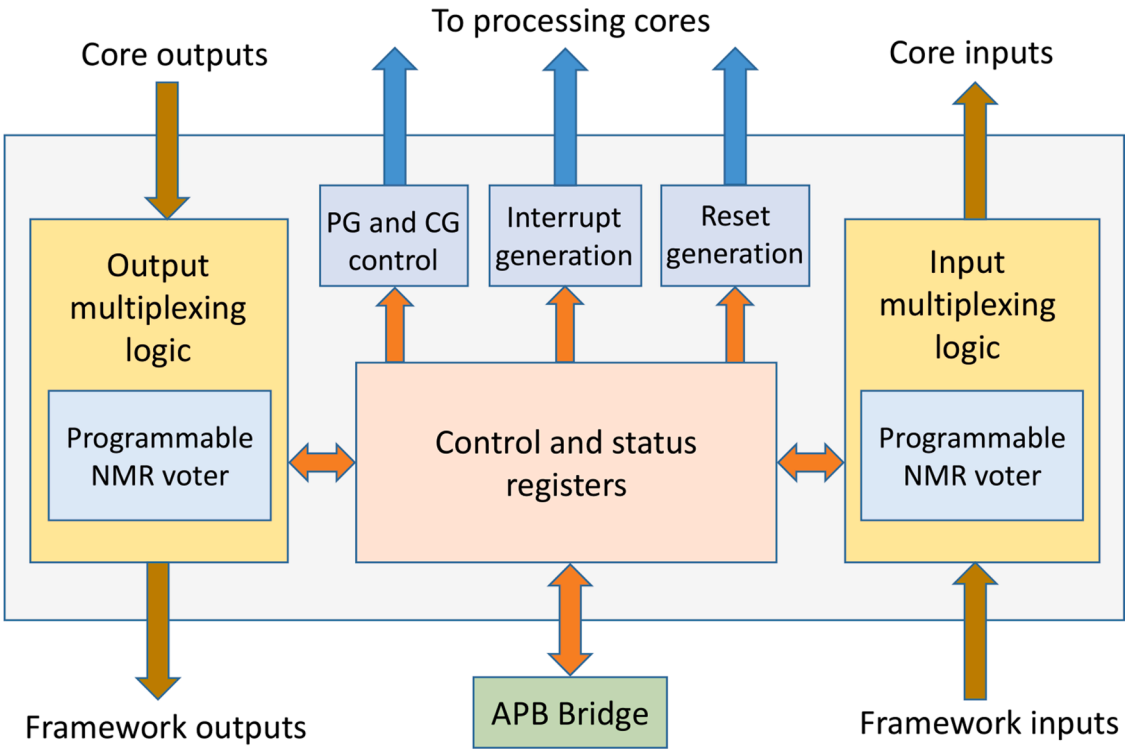

Fig. 11. *Waterbear* framework controller

approach offers the benefit of negligible hardware overhead, because most of already existing on-chip resources are reused for the SEU detection. A block diagram of the SRAM detector is presented in Fig. 12, and a detailed description of its design and functionality is given in [49].

The particle detection operates on the principle of detecting the bit-flips induced in the SRAM cells. Therefore, based on detected number of bit-flips and the SRAM cross-section obtained experimentally, the particle flux can be calculated. Standard error detection and correction (EDAC) and scrubbing mechanisms are employed to protect the memory against SEUs and detect single/double bit errors as well as permanent faults in each memory word. The counters are used to count the single/double bit errors and permanent faults, and the number of detected errors in each hour is saved in a register file. Based on the measured error rate, the *Waterbear* framework controller can activate appropriate fault-tolerant modes. The time required to scrub the entire memory is around 50 ms, which is sufficiently fast for detecting the particle flux in space. The proposed detector can be combined with a machine learning algorithm to predict the occurrence of solar particle events at least one hour in advance [50]. In order to enable the SEU rate prediction, a hardware accelerator needs to be added. A design of a hardware

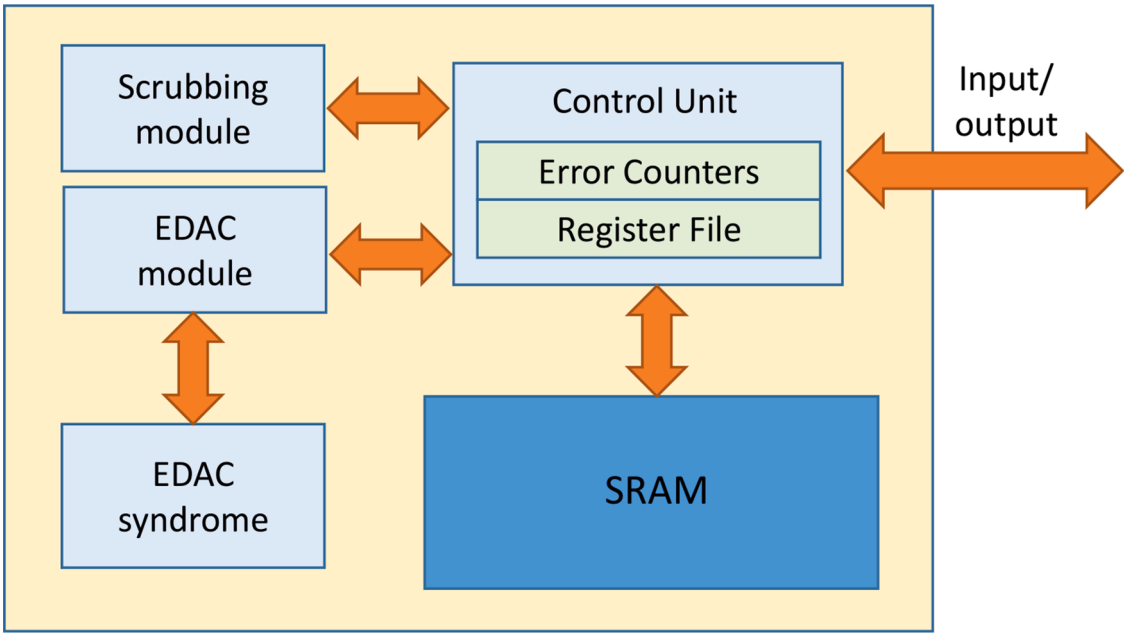

Fig. 12. Embedded SRAM for data storage and SEU rate detection

accelerator for SEU prediction with a linear regression machine learning model has been proposed in our previous work [51].

6.5 Aging Sensors

Aging effects lead to long-term degradation of transistors' characteristics, eventually resulting in increase of the input-output delay, and hence in degradation of system performance. In nanoscale CMOS technologies, the two most critical aging effects are the Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI). To mitigate these effects and increase the system lifetime, the aging monitor combining the NBTI and HCI sensors is required. In this case, the aging monitor based on two inverter chains (one for monitoring the NBTI, and the other for HCI), proposed in [52], was chosen. The main advantage of this monitor over other solutions is the simple design (based on digital standard logic cells and storing of aging information in the form of digital code). The aging information is used for controlling the de-stressing of the cores, thus allowing to extend the core lifetime, which is essential in long-term space missions.

6.6 Temperature Sensors

The on-chip temperature monitoring is important for the thermal management of the chip, since the operating temperature may vary depending on the workload. For this purpose, the *Proportional To Absolute Temperature* (PTAT) sensors are chosen. They work linearly in the range from - 55 to 125 °C giving a corresponding linear output in the range from 400 to 630 mV, i.e., with a slope of 1.29 mV/°C [17].

6.7 Peripheral Interface

Besides the readout interface for acquisition of data from the RADFET, several standard peripherals are included for interfacing with external hardware (e.g., memory, sensors, and processing units). The interfaces are: GPIO, Interrupt Request (IRQ) Controller, and Universal Asynchronous Receiver Transmitter (UART).

6.8 Radiation Hardening Measures for Digital Logic

The radiation hardness is a critical design requirement for the MPSoC. As we intend to implement the MPSoC with a standard CMOS technology, it is first necessary to evaluate the robustness of selected technology and corresponding standard cell library. The IHP's 130 nm bulk CMOS technology has been evaluated with extensive radiation tests. It was shown that MOS transistors are robust to total doses up to 500 Gy (50 krad), and with enclosed layout transistors (ELT) the total doses beyond 2000 Gy (200 krad) can be tolerated [53]. With this level of total dose tolerance, the selected technology may be suitable for conventional space applications (e.g., orbital satellites). However, like for any standard CMOS technology, the sensitivity to SEEs must be minimized with appropriate radiation-hardening-by-design measures.

Although the NMR configurations provide a high level of protection, it is still necessary to apply local hardening to the most critical combinational and sequential elements in order to ensure their functionality when the cores are operating in high performance mode. For example, an SET in a clock tree may propagate to multiple flip-flops and cause multiple bit-flips. Similarly, an upset in the control and reset logic may result in a Single Event Functional Interrupt (SEFI), i.e., multiple errors that may induce an undesired reset of the processing cores or SRAM, or initiate an undesired state. Thus, the SET filtering and TMR at the flip-flop level need to be applied selectively to the most sensitive gates. Our previous heavy ions experiments have shown that the custom-designed SET filters can suppress all SETs shorter than 500 ps, which covers most of the expected SET pulse widths in the investigated 130 nm technology. Furthermore, different variants of IHP's TMR flip-flops have shown immunity to SEUs up to the Linear Energy Transfer (LET) from 32.4 to 62.5 $MeVcm^2mg^{-1}$ [54]. This is sufficient as most particles in space have LET < 30 $MeVcm^2mg^{-1}$.

One of the most sensitive elements in the MPSoC is the SRAM, which may be sensitive to single and multi-bit upsets [55, 56], as well as to SEL and SEFI. As mentioned in Section 6.4, the standard EDAC and scrubbing mechanisms are employed to detect single and double upsets. However, this approach can correct only double upsets occurring in different memory words. In order to provide protection against multiple-bit errors in a single memory word, we aim to apply the well-known interleaving technique, i.e., distributing the memory cells from the same word into different columns, so that they are physically distant from each other. In such a way, the probability that a single particle hits multiple bits of the same word is reduced. We also aim to investigate the applicability of advanced coding techniques for detection and correction of multiple errors [57].

Special design measures have to be applied to ensure high tolerance to SEL. Heavy ion experiments have shown that the IHP's 130 nm standard cell library is latchup-free up to LET of 67 $MeVcm^2mg^{-1}$ [53]. However, due to the potentially hazardous impact of SEL, it is necessary to apply the preemptive measures. For this purpose, the SEL protection switch proposed in [58] is selected. It is a combinational circuit with a large PMOS transistor acting as SEL sensor. The operating principle is based on detection of excessive current flow and subsequent resetting of the power supply for the protected logic. The protection switch provides the power supply to the protected cells during normal operation, and switches off the power supply in the case of excessive supply current flow, i.e., when the SEL occurs. One SEL protection switch can protect tens to hundreds of logic cells, such that a complex design may require thousands of such switches distributed across the chip. The protection switches incur no area overhead because they are placed in empty cells beneath the power supply lines.

7. Preliminary Design Specifications

7.1 ASC Design Specifications

Design of ASC requires careful selection of components for the preprocessing of the voltage and current response of the RADFET under given radiation conditions. As the selection of analog components and their testing under radiation is ongoing work, here we will consider only the electrical design requirements. For that purpose, the experimental results for RADFET are used as a guide for defining the electrical specifications for current and voltage measurement.

As a case study, we have considered the experimental results for absorbed dose and dose rate measurement with the RADFET samples with 400 nm gate oxide, manufactured by Tyndall National Institute. The irradiation was performed with Co^{60} gamma radiation source, at the Vinca Institute of Nuclear Sciences, Belgrade, Serbia. Two sessions were conducted, one for measuring the threshold voltage shift in terms of total dose, and the other for measuring the induced current in terms of dose rate. The electrical response of the RADFETs was measured with a high precision source-measuring unit Keithley 2636A, controlled by a personal computer.

The threshold voltage shift was 15.6 V in zero-bias mode, for the total dose of 1330 Gy (133 krad). On the other hand, the currents from 190 pA to 4.1 nA have been measured for the dose rate from 0.5 to 32 Gy/h, with reverse bias of 10, 20 and 30 V. These results suggest that both the voltage and current measurement should be conducted over a wide dynamic range. However, it is important to note that the total doses measured in space missions may be lower than those obtained in terrestrial radiation experiments. For example, in KITSAT-1 satellite mission, the reported doses measured with two different RADFETs were 57 Gy (5.7 krad) and 32 Gy (3.2 krad) per year, while the maximum measured threshold voltage shift was below 3 V for a period of 800 days [8]. For a satellite lifetime of ten years, the total dose would be more than twice lower than that measured in our experiment.

In the ASC design, the most critical aspect is the low current measurement. As the radiation-induced current in the RADFET may be in the pA range, special design measures need to be adopted in order to measure accurately such low currents. It is required to use the ultra-low input bias current operational amplifiers for the transimpedance and current integrating stages. Typical example of a commercial rad-hard operational amplifier with ultra-low input bias current is LMP7704-SP from Texas Instruments. It has the input bias current of around 500 fA, which is lower than the expected radiation-induced current (above 100 pA). Besides the selection of appropriate amplifier, the printed circuit board should be designed to minimize the leakage currents. This can be achieved by routing the current from the sensor to the amplifier through a wire hanging in the air. Alternatively, the leakage current can be minimized by placing guard rings around the amplifier's input pins. Furthermore, proper shielding is essential to minimize the impact of external noise.

7.2 MPSoC Design Specifications

Since the proposed MPSoC design is based on previous designs [17, 49], the preliminary design specifications have been defined considering the previous implementation results. The specifications are given in Table 2. Almost 40 % of the area is occupied by the four LEON cores. The clock frequency of 50 MHz has been selected based on previous designs in the target technology, and we estimate that it is sufficient for the intended dosimetry application, because the voltage and direct current readout is generally a slow process, and even the pulsed current readout is not expected to have a high rate.

For data storage medium and particle detection, a 16 Mbit SRAM integrated in MPSoC has been selected. This choice is based on our previous analysis, which has shown that smaller SRAMs would not be suitable for detection of SEU rates at low radiation exposure. Namely, using smaller SRAMs would require longer measurement interval to acquire statistically meaningful data when the particle flux is low. It is possible to use larger SRAM if the area constraints are not violated.

For analog-to-digital conversion, an 8-channel 12-bit ADC has been chosen. Since the voltage and current measurement units have multiple ranges, the 12-bit ADC (with 4096 discrete levels) is sufficient for measuring the absorbed dose and dose rate in each range. Given that the maximum expected threshold voltage shift in dose measurement mode is around 15 V, it is possible to define three measurements ranges, where each range would cover an interval of 5 V. Thus, the resolution for each range would be 0.0012 V. In the case of current measurement, the overall range is divided into pA range and nA range. In the pA range, the expected resolution is 0.5 pA, while in the nA range the resolution is 10 pA.

As the irradiation results for the proposed design are still not available, preliminary estimate of radiation tolerance is based on prior experimental results presented in Section 6.8. Accordingly, we estimate that a chip designed in the selected 130 nm technology would be immune to SEL at least up to LET of 67 $MeVcm^2mg^{-1}$. Based on experimental results for IHP's TMR flip-flops, we estimate that the threshold LET for the entire system designed with these flip-flops would be at least 32.4 $MeVcm^2mg^{-1}$.

Table 2
MPSoC specifications

Parameters	Value
Core supply voltage	1.2 V
Pad supply voltage	3.3 V
Clock frequency	50 MHz
Processor area (4 LEON2 cores)	4×5.22 mm^2
SRAM area	14 mm^2
SRAM capacity	16 Mbit
ADC	12-bit
Peripherals area	< 20 mm^2
Total chip area	< 55 mm^2
Static power consumption	< 200 mW
SEU tolerance	> 32.4 $MeVcm^2mg^{-1}$
SEL tolerance	> 67 $MeVcm^2mg^{-1}$

7.3 MPSoC Power Consumption Analysis

As the energy resources are limited in space, it is important to assess the benefits of the self-adaptive multiprocessing in terms of power saving. In that regard, we have estimated analytically the power consumption of various operating modes of MPSoC for the period of one year. Since the self-adaptive functionality is primarily intended to protect the MPSoC under dynamic radiation conditions, such as those during an SPE, we have considered realistic SPEs measured in space. As a case study, we have analyzed all 36 SPEs during the solar cycle 24 (from 2008 to 2019). The particle flux for these SPEs has been measured with orbital satellites and the data is available online [59, 60]. Using the flux database and the computation methodology outlined in [50], we have computed the SRAM SEU rate for the whole year, taking the average of all SPEs.

Table 3 presents the calculated SRAM SEU rates in the solar cycle 24, corresponding operating modes, as well as the average hours for corresponding SEU rates in one year. According to the solar cycle conditions (i.e., solar maximum and solar minimum cycle), the background SEU rate of the target SRAM would be around 10^{-7} upsets/bit/day. We classify the SEU rate into four levels of criticality: "low", "medium", "high" and "very high". For example, the "low" level indicates the low radiation intensity, which cannot affect the functionality of the system. Thus, at "low" criticality level, the MPSoC can operate either in high-performance or de-stress modes. When SEU rate increases, it is classified into "medium", "high" and "very high" criticality levels, and accordingly the DMR, TMR and QMR fault-tolerant configurations are applied. When an SPE occurs, the SRAM SEU rate increases several times to thousands of times compared to the background level. As can be noticed, the highest SEU rates last very shortly (several hours or days), and this is typically the case for any SPE. Therefore, the highest level of protection would be required only for a short period.

Fig. 13 illustrates the power consumption of the MPSoC in one year, for different operating modes. For simplicity, we assume that the power consumption of one core per hour is the same for all operating modes. Thus, the total power consumption of one core per year, for a given operating mode, can be estimated as the product of the number of hours spent in that mode and the power consumption of one core per hour P. Accordingly, the total annual power consumption of the MPSoC, for the self-adaptive mode, can be calculated as $Power = 8556 \bullet P + 2 \bullet 142 \bullet P + 3 \bullet 43 \bullet P + 4 \bullet 19 \bullet P = 9045 \bullet P$. As can be observed, compared with the static core-level NMR fault-tolerant modes, the power consumption in the self-adaptive mode is much lower. By static NMR modes we mean that only a particular NMR mode (DMR, TMR or QMR) is employed when the radiation protection is required. The results show that the power consumption in the self-adaptive mode is twice lower than in the static DMR mode, almost 3 times lower than in the static TMR mode, and almost 4 times lower than in the static QMR mode.

8. MPSoC SER Monitoring

To enable the autonomous selection of fault-tolerant modes for the

Table 3
Hours per year spent in different operating modes according to the SEU rate (upsets/bit/day)

Criticality level	SEU rate	Operating mode	Hours / year
Low	$< 10^{-6}$	High performance or destress	8556
Medium	$10^{-6} - 10^{-5}$	DMR	142
High	$10^{-5} - 10^{-4}$	TMR	43
Very high	$> 10^{-4}$	QMR	19

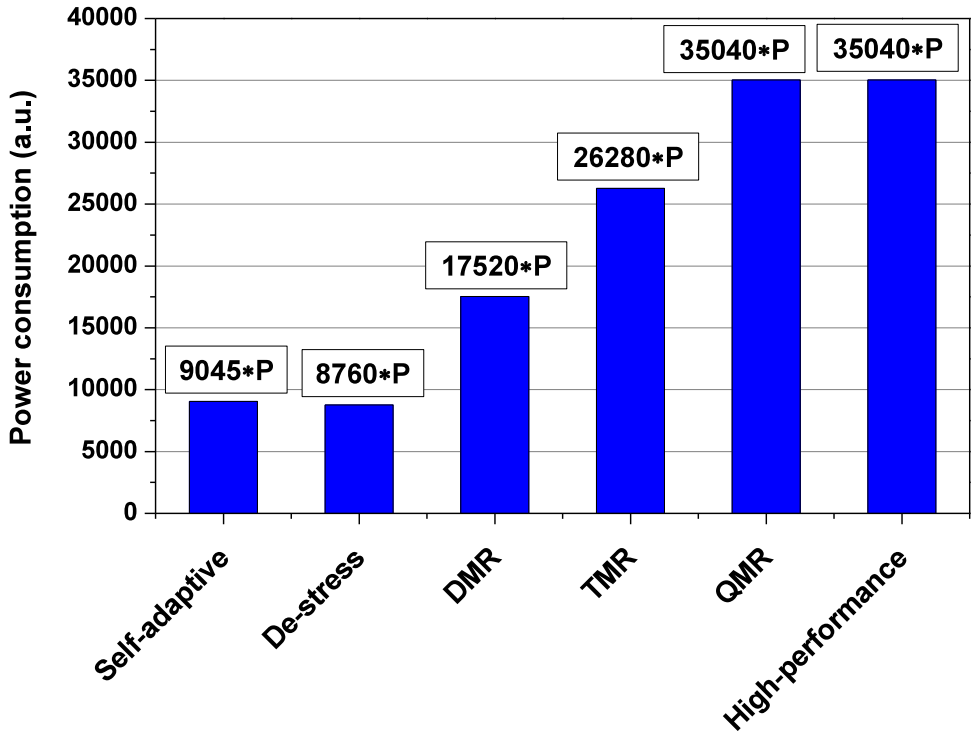

Fig. 13. Estimated annual power consumption for different operating modes of MPSoC, based on the average of all SPE data for the period from 2009 ro 2018

MPSoC, the on-line monitoring of its SER is mandatory. As the SER is dependent on numerous contributing parameters, it may vary over a wide range during a typical space mission. Therefore, it is necessary to monitor continuously all relevant parameters affecting the SER. In this case, we consider the dependence of SER on six parameters: particle flux, supply voltage, temperature, clock frequency, aging and total dose. It is

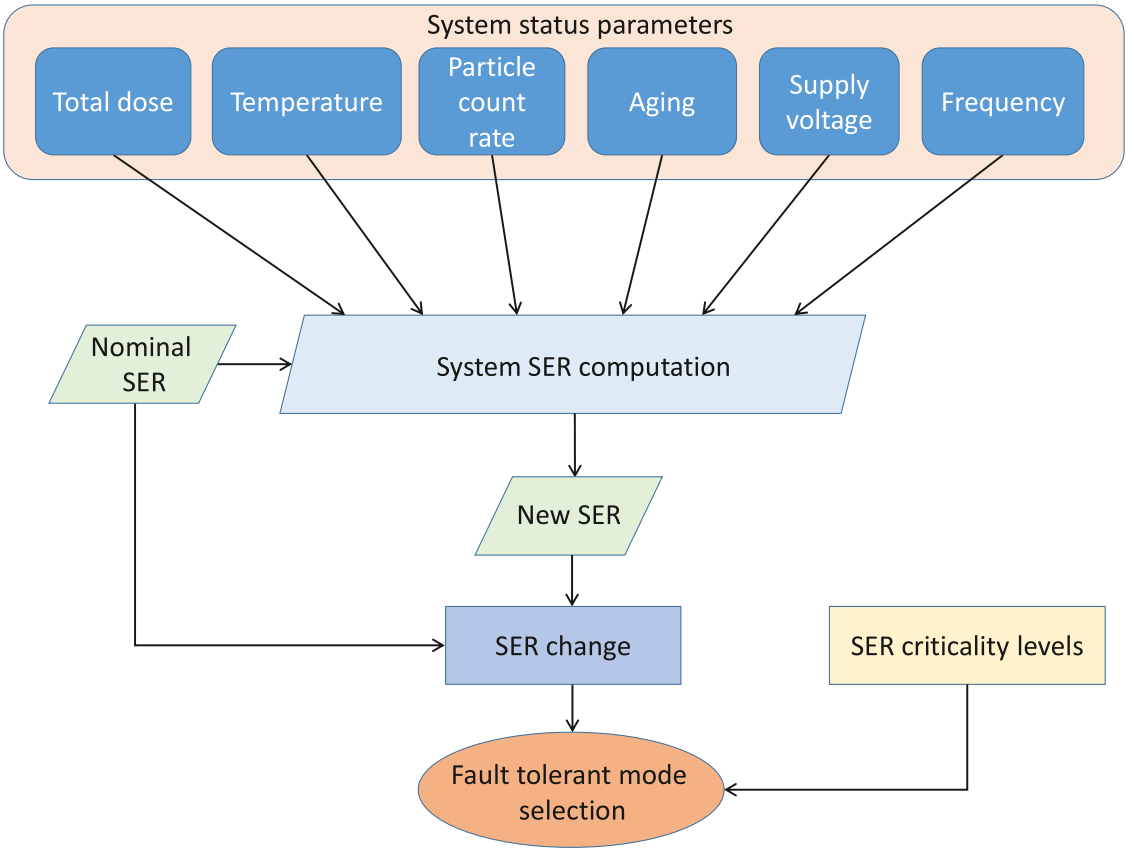

Fig. 14. Online SER monitoring based on collaborative sensing of system status parameters

important to consider jointly the aforementioned parameters because, as mentioned in Section 2, neglecting the contribution of any of them would result in prohibitively high errors in the SER computation. The total dose is measured with external sensor (RADFET), while all other parameters are measured with the sensors embedded in MPSoC. The acquired data is then utilized to calculate the actual SER. A general flow for the online monitoring of SER variation is illustrated in Fig. 14. It is important to note that besides the aforementioned parameters, the SER also depends on the operating state of the core (i.e., the program executed by the core), because different operating states may result in different logic levels within the circuit, and thus in different sensitivity of logic gates.

The main idea of the SER monitoring flow depicted in Fig. 14 is to assess the SER variations of each core in real time, based on the executed tasks and six contributing parameters measured by the sensors. The actual (measured) SER, denoted as *New SER* in Fig. 14, is compared with the *Nominal SER*. To optimize the usage of processing resources, the computation is done only when significant changes of the sensors' readout are detected. The difference between *New SER* and *Nominal SER* values, denoted as *SER change* in Fig. 14, is compared with the predefined SER criticality levels, and appropriate actions are triggered to set the required mode. The *Nominal SER* is determined in the system design phase, for the predefined values of flux, supply voltage, temperature and clock frequency, without aging and total dose effects. As the SER depends on operating scenario of the processor, a set of *Nominal SER* values are determined for different states, and stored in look-up tables. Similar procedure is then applied to determine the expected SER values (*New SER*) for different combinations of operating scenarios and different values of the contributing parameters that will in practice be measured with sensors. As a result, another set of look-up tables is constructed to store the expected SER values. These look-up tables are stored in the MPSoC and the data is used to evaluate the SER changes during the mission. As the look-up tables cannot store all possible combinations of parameters, the interpolation is employed to determine the missing values.

In general, the SER of a complex system is the sum of the SER values of all components (logic elements) in the system. To determine the SER of each component, the soft error generation probability and derating (masking) factors have to be calculated. Numerous methods for SER calculation have been proposed in literature, but this is beyond the scope of this work. We intend to perform detailed SER analysis once the MPSoC design is finalized. Choice of appropriate SER computation methodology depends on the complexity of the design, and involves the combination of simulation-based and analytical evaluation methods, and a limited number of irradiation experiments.

This work introduces a design concept for a radiation hardened RADFET readout system, combining the simultaneous monitoring of absorbed dose and dose rate with a self-adaptive quad-core processing platform. In comparison to the existing RADFET dosimeters, the presented solution provides higher level of integration with more efficient utilization of available resources. Simultaneous measurement of absorbed dose and dose rate eliminates the need for traditional dose rate sensors, such as diodes, thus reducing the design cost. The multi-core platform enables to control multiple radiation sensors or other types of sensors, as well as to implement additional tasks on the same chip, with dynamic adaptation to environmental conditions. As a result, a trade-off between performance, power consumption and fault tolerance can be maintained in real time. The following tasks are the implementation of proposed design and its verification with radiation experiments.

9. Conclusions

This work introduces a design concept for a radiation hardened RADFET readout system, combining the simulta-neous monitoring of absorbed dose and dose rate with a self-adaptive quad-core processing platform. In comparison to the existing RADFET dosimeters, the presented solution provides higher level of integration with more efficient utilization of available resources. Simultaneous measurement of absorbed dose and dose rate eliminates the need for traditional dose rate sensors, such as diodes, thus reducing the design cost. The multi-core platform enables to control multiple radiation sensors or other types of sensors, as well as to implement additional tasks on the same chip, with dynamic adaptation to environmental conditions. As a result, a trade-off between performance, power consumption and fault tolerance can be maintained in real time. The following tasks are the implementation of proposed design and its verification with radiation experiments.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could influence the work presented in this paper.

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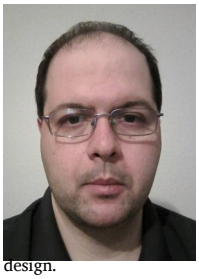

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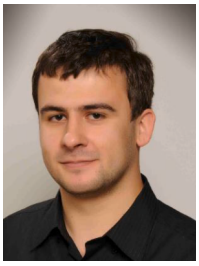

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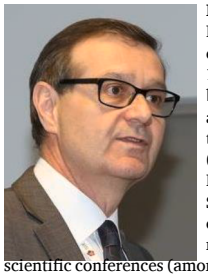

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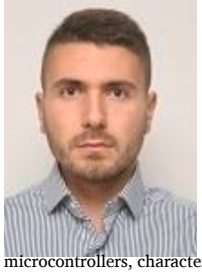

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